****

**FIRST SEMESTER 2019 – 2020**

**COURSE HANDOUT (PART II)**

01-08-2019

In addition to Part I (General Handout for all courses appended to the timetable) this handout gives further details regarding the course.

*Course No* : **CS F342**

*Course Title* : **Computer Architecture**

*Instructor-in-charge* : **Prof. G Geethakumari**

*Instructors* : Suvadip Batabyal

**1. Scope and Objective of the Course:**

The scope of this course is to cover various aspects of Computer Architecture, which is a specification detailing how a set of software and hardware technology standards interact to form a computer system or platform. Performance issues with respect to computer system design and the compatible technologies would be discussed.

The main objective of this course is to give the students exposure to

* Processor performance criteria, performance benchmarks
* CPU design - instruction set architecture, instruction execution
* Single and Multicycle implementation, ILP, Pipeline design, Hazards
* Methods of overcoming hazards, Branch prediction
* Memory subsystems including cache optimization

**2. Text Book:**

T1. Patterson, D.A. & J.L. Hennessy, Computer Organization and Design: MIPS Edition, Elsevier, 5th edition., 2013.

**3. Reference Books:**

(i)Hamacher et. al, Computer Organisation, McGraw Hill, 5th ed., 2002.

(ii)J.L. Hennessy & D.A. Patterson, Computer Architecture: A Quantitative Approach, Morgan Kauffmann, 5th Ed, 2012.

(iii)W. Stallings, Computer Organisation & Architecture, PHI, 6th ed., 2004.

(iv) Additional material to be put up in CMS

**4. Course Plan:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Lecture No.** | **Learning Objectives** | **Topics to be covered** | **Chapter in the Text Book** |
| 1 - 2 | To understand about the overview of classes of computers | Computer Abstractions and Technology | Ch. 1 |
| 3 - 4 | To learn about instructions; ISA as well as know about sample ISAs like MIPS | Instructions- language of the computer | Ch.2 |
| 5-7 | MIPS Architecture & Instruction Set | Ch. 2 |
| 8 |
| 9 - 11 | To practice arithmetic operations on integers; floating point numbers etc | Arithmetic for computers: floating point arithmetic | Ch 3 |
| 12 -13 | To understand the basics of processor; learn about data path, control path | Processors: logic design conventions | Ch 4 |
| 14 - 15 | Role of Performance, pipelining – design issues | Ch 4 |
| 16 - 17 | Pipelined data path and control | Ch 4 |
| 18 | Various types of hazards | Ch 4 |
| 19 | Structural hazards | Ch 4 |
| 20 - 21 | Data Hazards | Ch 4 |
| 22 - 23 | Control Hazards | Ch 4 |
| 24 | Branch prediction techniques | Ch 4 |
| 25 | Static Branch Prediction | Ch 4 |
| 26 | Dynamic Branch Prediction | Ch 4 |
| 27 | To know about the organization of memory hierarchy and learn various optimization techniques at each level | Exploiting memory hierarchy - introduction | Ch 5 |
| 28 | Cache Memory Organization | Ch 5 |
| 29-32 | Measuring and improving cache performance, cache optimization | Ch 5 |
| 33 - 34 | Main Memory and Interleaving | Ch 5 |
| 35 | Virtual Memory and Virtual Machines | Ch 5 |
| 36-38 | Performance and memory hierarchies: Cache coherence | Ch 5 |
| 39 | To understand about storage systems and performance | Storage and other I/O topics | T1 Ch5; R(ii) |
| 40 | Dependability, reliability, availability | T1 Ch5; R(ii) |
| 41 - 42 | I/O performance measures, Redundant Array of Independent Disks | T1 Ch5; R(ii) |

**5. Evaluation Scheme:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **EC No.** | **Evaluation Component** | **Duration** (Min) | **Weightage** **(%)** | **Date** **& Time** | **Nature of Component** |
| 1 | Mid Sem Test | 90 | 30 | 1/10, 3.30 -- 5.00 PM | Closed Book |
| 2 | Quizes (4Nos.)  +  Lab tests (4 Nos.)  (to be conducted together in the lab) |  | 10 %  +  20% |  | Open Book |
| 3 | Comprehensive | 180 | 40 | 7/12 AN | Closed Book |

**6. Chamber Consultation Hour:** To be announced in the class

**7. Notices:** Notices regarding the course will be put up on the CSIS notice board and in CMS.

**8**. **Makeup Policy:** No makeup exam allowed without prior permission. For lab evaluation component, there is no makeup.

9**. Academic Honesty and Integrity Policy:** Academic honesty and integrity are to be maintained by all the students throughout the semester and no type of academic dishonesty is acceptable.

INSTRUCTOR-IN-CHARGE